

Address	A19	A17	A15	HEX Addr
ROMA	0	0	0	0x00000
ROMB	0	0	1	0x08000
Screen0	0	1	0	0x20000
Screen1	0	1	1	0x28000
	1	0	0	0x80000
	1	0	1	0x88000
ROMC	1	1	0	0xA0000
ROMD	1	1	1	0xA8000

74LS138 on CPU Board – A19, A17 and A15 wired to C,B and A, A18 and A16 wired to /G1 and /G2 enables, hi enable wired to 5V via resistor. Only Y0, Y1, Y6 and Y7 are wired to ROM's /CE pins

Only Y6 and Y7 drive /DTACK gated with /DS - /DTACK for the lower ROM's is from ZX8301

Address	19	18	17	16	15	Y	
0x00000	0	0	0	0	0	0	1st 32K OS ROM - the 2 socket footprints also have
0x08000	0	0	0	0	1	1	2nd 32K OS ROM – these 2 ROMS as 64K space
0x10000	0	0	0	1	x		ZX8302 ULA Space 64K
0x20000	0	0	1	0	0	2	First Video Screen
0x28000	0	0	1	0	1	3	Second Video Screen – not used on OPD
0x30000	0	0	1	1	x		64K DRAM
0x40000	0	1	0	0	0		16K ULA3 A14 Low
0x44000	0	1	0	0	0		2K CMOS RAM
0x44800	0	1	0	0	0		6K I/O Area
0x46000	0	1	0	0	0		8K reserved
0x48000	0	1	0	0	1		32K 4 slot ROM pack
0x50000	0	1	0	1	0		Reserved 32K – unusable – echo of 40000-47FFF
0x58000	0	1	0	1	1		32K 4 slot ROM pack
0x60000	0	1	1	0	0		Reserved 32K – unusable – echo of 40000-47FFF
0x68000	0	1	1	0	1		32K 4 slot ROM pack
0x70000	0	1	1	1	0		Reserved 32K – unusable – echo of 40000-47FFF
0x78000	0	1	1	1	1		32K 4 slot ROM pack
0x80000	1	0	0	0	0	4	32K ROM Expansion – this appears to be the 128K RAM
0x88000	1	0	0	0	1	5	32K ROM Expansion – expansion too
0x90000	1	0	0	1	0		64K - this also part of the 128K RAM expansion area
0xA0000	1	0	1	0	0	6	3 rd 32K OS ROM
0xA8000	1	0	1	0	1	7	4 th 32K OS ROM
0xB0000	1	0	1	1	0		64K – but usable as ROM space if decoded
0xC0000	1	1	0	0	0		144K Exchange ROM and add ons (ROM Pack)
0xE8000	1	1	1	0	1		32K ROMCAP J1
0xF0000	1	1	1	1	0		32K ROMCAP J2
0xF8000	1	1	1	1	1		Reserved

	A1	C1	
	A2	C2	
	A3	C3	A13 on J2
0V	A4	C4	0V
A3	A5	C5	A2
A4	A6	C6	A1
A5	A7	C7	A0
A6	A8	C8	FC0
A7	A9	C9	FC1
A8	A10	C10	FC2
A9	A11	C11	/IPL0-2
A10	A12	C12	/IPL1
A11	A13	C13	/BERR
A12	A14	C14	/VPA
A13	A15	C15	E
A14	A16	C16	/RESET
A15	A17	C17	CLK
A16	A18	C18	/BR
A17	A19	C19	/BG
A18	A20	C20	/DTACK
A19	A21	C21	R/W
D7	A22	C22	/DS
D6	A23	C23	/AS
D5	A24	C24	D0
D4	A25	C25	D1
D3	A26	C26	D2
/HALT	A27	C27	A19 Inverted
	A28	C28	EXTINTL
BAUDX4 (ZX8302)	A29	C29	RESETIN
	A30	C30	
	A31	C31	Pin 20 TMS5220 - TEST
5V	A32	C32	5V

64 PIN A/C row expansion bus – middle row B has about 5 ground pins spaced out

ROM Pack buffers address and control signals through LS244 buffers, and data through LS245 (R/W) gates direction.

PLA consumes A19-A15 (on pins 6 thru to 2), and decodes 5 x 32K ROMs on B0-B4 outputs, /DSL gates /OE. B5 drives ROM slot 0 (J1) , B6 drives ROM slot 1 (J2) , also B7 (input) appears on Slot 1, B8 drives /G on the LS245 data transceiver, and B9 drives /DTACK.

The PLA Pinout is as follows:

/VPA	1	20	5V
A15	2	19	/DTACK
A16	3	18	/G on LS245 Data Transceiver
A17	4	17	J2 Slot1 pin 27
A18	5	16	J2 Slot 1 /CE - pin 15
A19	6	15	J1 Slot 0 /CE – pin 15
/AS	7	14	/ROM4
J1 Slot0 pin 27	8	13	/ROM3
/ROM0	9	12	/ROM2
0V	10	11	/ROM1

4 Slot PLA:

/AS	1	20	5V
A15	2	19	J4 Slot0 pin 27
A16	3	18	J5 Slot0 pin 27
A17	4	17	/DTACK
A18	5	16	/G on LS245 Data Transceiver
A19	6	15	J5 /CE – pin 15
J2 Slot0 pin 27	7	14	J4 /CE – pin 15
J3 Slot0 pin 27	8	13	J3 /CE – Pin 15
/ROM0	9	12	J2 /CE – pin 15
0V	10	11	/ROM1

The connections for the ROM slot headers are as follows:

A14	1	2	5V
A13	3	4	A12
A8	5	6	A7
A9	7	8	A6
A11	9	10	A5
/OE (/DS)	11	12	A4
A10	13	14	A3
/CE (from PLA)	15	16	A2
D7	17	18	A1
D6	19	20	A0
D5	21	22	D0
D4	23	24	D1
D3	25	26	D2
Slot Enable (to PLA)	27	28	R/W
C28 'EXTINTL' ULA3	29	30	0V

32 pin Expander (telecoms module)

(This is mostly reverse engineered).

5V	A1	C1	5V
4k7 pin 15 8051	A2	C2	Pin 27 ULA3 (INT0)
Pin 25 ULA3 (T1)	A3	C3	Clear LS175 (7910-3) **
Pin 24 ULA3 (P3.6 WR)	A4	C4	NC
NC	A5	C5	0V
Pin 26 ULA3 (P3.7 RD)	A6	C6	KBD Parallel load (P1.3)
Pin 21 8051 (Hook Sw)	A7	C7	KBD Shift out (P1.2)
KBD 10 (P0.0)	A8	C8	SW1.1
KBD 9 (P0.1)	A9	C9	Unused – link to A10)
KBD Shift Clock (P1.0)	A10	C10	NC
KBD Shift in (P1.1)	A11	C11	NC
B_4052 pin 11	A12	C12	0V
A_4052 pin 3	A13	C13	NC
A_4052 pin 15	A14	C14	NC
Clear LS164 (5V)	A15	C15	NC
Modem sound out	A16	C16	NC

** is reset for modem and LS175 – from ZX8302 reset out

P2.3-P2.0 are D3-D0 for DTMF Tone generator, D4 is P2.4, P2.6 is strobe (PCD3311)

P2.6 decodes expander – 82c43, P2.5 is Prog P4-0-3 for MC0-3, MC4 is P5.0 (modem control on 7910) , P5.1 is DTR, P5.2 is RTS, P5.3 is BRTS, P6.0 is CD, P6.1 is CTS

P7.3 is B select IC6, P7.2 is A P1.4 is A on IC4, P1.5 is B P1.6 is A on IC5, P1.7 is B

P7.0 is 7 on ULN2001 via resistor (controls RL101) – other channels not yet decoded.

IC19 and IC 20 on the main board are 28 pin ROM sockets wired exactly the same way as QL ROM Sockets – driven by ZX8301. ZX8302 is wired the same as Issue 5 QL (so sits on the video data bus)

ZX8302 – EXTINT is wired to R15 (from 5V) / Q6 – Q6 driven from Battery test circuit. QL Network is brought out to 2 pads near the chip One serial port on the ZX8302 drives the RS432 printer port (out only)

COMDATA is used as a clock for LS175, and data is from MDSELDN. The LS175 controls LED's and MOSFET switches for the telephone part of the unit Addresses appear to be the same for on board registers for ZX8302 and ZX8301.

ZX8302 Interrupt is wired to for Interrupt level 2, and the same FC0 / FC1 gated to VPA used for autovectored.

ULA 3 is a logic array of some sort but not complicated (it is registered)

D0	1	28	5V
D1	2	27	C2 on 32 connector (INT0)
D2	3	26	A6 on 32 connector (RD)
D3	4	25	A3 on 32 connector (T1)
A13	5	24	A4 on 32 connector (WR)
A14	6	23	/CE1 on 2K CMOS via logic
A15	7	22	IPL2/IPL0
A18_A19	8	21	INT_C28
/DS	9	20	IPL1
/DSMC_A19	10	19	INT Speech
A1	11	18	WS Speech
A0	12	17	RS Speech
R/W	13	16	READY Speech
OV	14	15	/DTACK

Assumptions – D0-D3 are used with addressing to decode the 4 speech I/O control lines, and the 4 control lines going to the telecom module on the 32 pin connector.

Simple addressing decodes these 2 registers above (the latter may be bi directional?), and decodes for DSMC and the 2K RAM. A19 is used with NAND gate externally to gate DSMC and A18 input.

The 2K CMOS RAM is powered from the Lithium cell or the 9V Battery??, and the /CE2 is tied to R25 and FT5 FET, presumably to prevent access to the RAM if voltage is unstable.

/CE1 on the 2K CMOS RAM is gated with FC2 – presumably to only allow access in supervisor mode to protect the contents

VCC for CMOS RAM – via D16 Lithium, 5V via D17

9v to R12, D13 & Q1 – difficult to find where this 9v goes – but It passes through the relay and several transistors – but can't track it to powering the CMOS RAM – I presume it's powering the ZX8302 through pin 40.

Powerdown Pin 14 on the 15 way D connector feeds the gates of most of the FET's on the main board and control the power to the board. Note from elsewhere say this must be held at +5V for normal operation.

/BERR pin 13 of 74LS123 1Q output, /DS gates pin 2, CPU CLK pin 1, reset clears the timer – any address that's accessed that hasn't provided DTACK – will generate this error. Therefore – any plugin ROM packs, extensions must assert DTACK.

The keyboard is handled by 2 shift registers. These are 74LS164 and 74LS165 respectively. The 74LS165 handles the 8 Y inputs from the matrix, the 74LS164 drives the 8 X outputs via diodes. There are 2 additional X lines that are not fed by the shift register – these drive the numeric keypad matrix keys that would be used for the telephone dialler. The following table outlines the key matrix:

	X1	X2	X3	X4	X5	X6	X7	X8	9	10
Y1	1 !	2 @ ©	3 £ #	4 \$	5 % \	6 ^ ~	7 & {	8 * }	'1'	'9'
Y2	TAB	Q	W	E	R	T	Y	U	'2'	'0'
Y3	Ins Del	A	S	D	F	G	H	J	'3'	ESC/*
Y4	L/R Shift	Z	X	C	V	B	N	M	'4'	PRT/#
Y5	9 ([0)]	Start	Resume	Review	Last Redial	Auto SPKR	List Recall	'5'	
Y6			I	O	P	_ -	+ =		'6'	
Y7	K	L	: ;	" '	Enter	< ,	> .	? /	'7'	
Y8	CTRL	←	→	Space	↑	↓		ALT	'8'	

Grey = unused element

Yellow = Blocking Diode